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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,910	04/16/2004	Byung Tai Do	27-017	8877

22898 7590 06/17/2005

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,910	DO ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to amended claims 1-20, filed 05/28/2005, have been considered but they are moot in view of new ground(s) of rejection.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "connecting the first die to the substrate uses a number of bonding wires; and attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires" of **claims 2 and 12** where "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"; and the "attaching a heat sink attaches a heat sink that has an electrically conductive coating ...connecting the electrically conductive coating to a ground plane" of **claims 4, 9, 14, and 19** where "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1,2,5-7,10-12,15-17 and 20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Akram U.S. Patent 6,351,028 (the '028 patent, which was cited in a previous office action) in view of Ho et al. U.S. Patent 6,507,104 (the '104 patent).

Referring to **claims 1, 6, 11, and 16**, the '028 patent discloses in Figures 2-9, particularly Fig. 7, and respective portions of the specification a semiconductor package, a method of using, and a method of assembling thereof, comprising:

providing a substrate (22);

attaching a first die (24) to the substrate;

electrically connecting the first die to the substrate;

attaching a heat sink (26, column 3, lines 61-67, "transfer of thermal energy or heat from semiconductor devices in contact with or around T-interposer 26") having an undercut around its periphery to the first die;

attaching a second die to the heat sink;

electrically connecting the second die to the substrate; and

encapsulating (Fig. 7, using epoxy 50) the first die, the heat sink, and the second die.

However, the reference fails to teach that the heat sink includes a plurality of legs integrally formed with the undercut portion of the heat sink, and thus further fails to teach attaching the plurality of legs to the substrate.

Ho - in also disclosing, in Fig. 2, a semiconductor package, a method of using, and a method of assembling thereof comprising a substrate 21, a semiconductor die 22 ("semiconductor chip"), a heat sink 20 having a body portion ("flat portion" 200) and an undercut around its periphery and a plurality of legs ("supporting portion" 201) integrally formed with the undercut portion of the heat sink, the plurality of legs attached to the substrate – teaches that the plurality of legs provide support for the body portion to be positioned above the semiconductor die.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '028 patent' heat sink such that the heat sink has a plurality of legs integrally formed with the undercut portion of the heat sink. One would have been motivated to make such a change so that the plurality of legs provide support for the body portion which is positioned above the semiconductor die, as taught by the '104 patent. A semiconductor package such modified hereinafter is referred to as the '028/104 device, and the combined teachings is referred to as the '028/104 reference.

Referring to **claims 2, 7, 12, and 17**, the '028/104 reference further discloses electrically connecting the first die (24) to the substrate uses a number of bonding wires (no number) and attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires, that extends laterally over the lower die, and such that the undercut of the heat sink extends laterally over the number of bonding wires.

Referring to **claims 5 and 15**, as evident from Figs. 5 and 9 of the '028 reference, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die.

Referring to **claims 10 and 20**, as evident from Fig. 7, the reference further discloses providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies.

4. **Claims 3, 8, 13, and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over Akram U.S. Patent 6,351,028 (the '028 patent) in view of Ho et al. U.S. Patent 6,507,104 (the '104 patent) as applied above (the '028/104 reference) and further in view of Chiu et al. U.S. Patent 6,437,984 (the '984 patent, cited in a previous office action).

The '028/104 reference discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, but fails to disclose that the heat sink is electrically grounded. Chiu, in disclosing a thermally enhanced chip scale package having a heat sink (114, Fig. 1B), teaches that the heat sink may be wire bonded to a ground connection to provide the packaged integrated circuit with shielding from electrical or electromagnetic interference (column 2, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the

'028/104 reference's heat sink so that the heat sink is electrically grounded using wire bonding. One would have been motivated to make such a modification in view of the teachings by Chiu that ground connection using wire bonding provide the packaged integrated circuit with shielding from electrical or electromagnetic interference. A semiconductor package such modified hereinafter is referred to as the '028/104/984 device, and the combined teachings is referred to as the '028/104/984 reference.

5. **Claims 4, 9, 14, and 19** are rejected under 35 U.S.C. §103(a) as being unpatentable over Akram U.S. Patent 6,351,028 (the '028 patent) in view of Ho et al. U.S. Patent 6,507,104 (the '104 patent), further in view of Chiu et al. U.S. Patent 6,437,984 (the '984 patent) as applied above (the '028/104/984 reference), and further in view of Shin et al. U.S. Patent 5,854,511 (the '511 patent, cited in a previous office action).

The '028/104/984 reference discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, 3, 8, 13, and 18, but fails to disclose that the heat sink has an electrically conductive coating connected to a ground plane on the substrate and consequently fails to teach that the second die is connected to the electrically conductive coating.

The '511 patent, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat sink of the '028/104/984 reference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a modification in view of the teachings by the '511 patent that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package. Thus the final modified package would have a heat sink having an electrically conductive coating connected to a ground plane on the substrate and that the second die would be connected to the electrically conductive coating as the second die is connected to the heat sink which has the electrically conductive coating, in order to achieve an improvement in performance of the finally produced semiconductor package.

6. **Claims 1,2,5-7,10-12,15-17 and 20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho et al. U.S. Patent 6,507,104 (the '104 patent) in view of Akram U.S. Patent 6,351,028 (the '028 patent, cited in a previous office action).

Referring to **claims 1, 6, 11, and 16**, the '104 patent discloses in Figure 2 and respective portions of the specification a semiconductor package, a method of using, and a method of assembling thereof, comprising:

providing a substrate (21);

attaching a first die (22) to the substrate;

electrically connecting the first die to the substrate;

attaching a heat sink (20, column 1, last paragraph) to the first die;

the heat sink comprising a body portion ("flat portion" 200), an undercut portion around a periphery thereof, and a plurality of legs ("supporting portions" 201) integrally formed with the undercut portion having an undercut around its periphery to the first die;

attaching the plurality of legs to the substrate; and

encapsulating the first die and the heat sink.

However, the reference fails to teach that the package comprises a second die, and thus fails to teach attaching a second die to the heat sink and electrically connecting the second die to the substrate.

Akram - in also disclosing a semiconductor package, a method of using, and a method of assembling thereof as detailed above – teaches forming a plurality of integrated circuit devices such as first die 24, second die 24, and third die 24 alternating with heat sinks 26, within a common package for increased semiconductor device density (column 2, lines 50-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '104 patent' package such that the package comprises a second die so as to achieve increased density. A semiconductor package such modified hereinafter is referred to as the '104/028 device, and the combined teachings is referred to as the '104/028 reference, and a process for forming such a modified semiconductor package would comprise attaching the second die to the heat sink and electrically connecting the second die to the substrate.

Referring to **claims 2, 7, 12, and 17**, the '104/028 reference further discloses electrically connecting the first die (24) to the substrate uses a number of bonding wires (no number) and attaching the modified heat sink attaches the modified heat sink that extends laterally over the

number of bonding wires, that extends laterally over the lower die, and such that the undercut of the heat sink extends laterally over the number of bonding wires.

Referring to **claims 5 and 15**, as evident from Figs. 5 and 9 of the '028 reference, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die.

Referring to **claims 10 and 20**, as evident from Fig. 7 of the '028 reference, the reference further discloses providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies.

7. **Claims 3, 8, 13, and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho et al. U.S. Patent 6,507,104 (the '104 patent) in view of Akram U.S. Patent 6,351,028 (the '028 patent) as applied above (the '104/028 reference) and further in view of Chiu et al. U.S. Patent 6,437,984 (the '984 patent).

The '104/028 reference discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, but fails to disclose that the heat sink is electrically grounded. Chiu, in disclosing a thermally enhanced chip scale package having a heat sink (114, Fig. 1B), teaches that the heat sink may be wire bonded to a ground connection to provide the packaged integrated circuit with shielding from electrical or electromagnetic interference (column 2, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '104/028 reference's heat sink so that the heat sink is electrically grounded using wire bonding. One would have been motivated to make such a modification in view of the teachings by Chiu

that ground connection using wire bonding provide the packaged integrated circuit with shielding from electrical or electromagnetic interference. A semiconductor package such modified hereinafter is referred to as the '104/028/984 device, and the combined teachings is referred to as the '104/028/984 reference.

8. **Claims 4, 9, 14, and 19** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho et al. U.S. Patent 6,507,104 (the '104 patent) in view of Akram U.S. Patent 6,351,028 (the '028 patent), further in view of Chiu et al. U.S. Patent 6,437,984 (the '984 patent) as applied above (the '104/028/984 reference), and further in view of Shin et al. U.S. Patent 5,854,511 (the '511 patent).

The '104/028/984 reference discloses a semiconductor package with stacked dies and a method of assembling and using thereof as claimed and as detailed above for claims 1, 6, 11, and 16, 3, 8, 13, and 18, but fails to disclose that the heat sink has an electrically conductive coating connected to a ground plane on the substrate and consequently fails to teach that the second die is connected to the electrically conductive coating.

The '511 patent, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat sink of the '104/028/984 reference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a

modification in view of the teachings by the '511 patent that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package. Thus the final modified package would have a heat sink having an electrically conductive coating connected to a ground plane on the substrate and that the second die would be connected to the electrically conductive coating as the second die is connected to the heat sink which has the electrically conductive coating, in order to achieve an improvement in performance of the finally produced semiconductor package.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTH

Tu-Tu Ho
June 12, 2005